AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A level converter for interfacing [[two]] circuits supplied by different supply voltages, said level converter comprising:

a first buffer receiving an input [[signal]], said first buffer being connected between a virtual supply and a supply return;

a second buffer receiving an output of said first buffer, connected between a first supply and said supply return; and

a supply select between said first supply and said virtual supply, said supply select receiving an output from said second buffer and selectively passing a first supply voltage on said first supply or a reduced supply voltage to said virtual supply [[line]] responsive to said output from said second buffer, said reduced supply voltage being such that standby power is eliminated in said first buffer when said input is high ~~output~~.

2. (original) A level converter as in claim 1, wherein said second buffer is an inverter.

3. (original) A level converter as in claim 1, wherein said supply select is a supply switch in parallel with at least one diode, both connected between said first supply and said virtual supply.

4. (original) A level converter as in claim 3, wherein said supply switch is a field effect transistor (FET) gated by said output of said second buffer and said at least one diode is a diode connected FET.

5. (original) A level converter as in claim 4, wherein said supply switch FET is a P-type FET (PFET) and said at least one diode connected FET an N-type FET (NFET) diode.

6. (original) A level converter as in claim 5, wherein said at least one diode connected NFET is a pair of series connected NFET diodes.

7. (original) A level converter as in claim 5, wherein said second buffer is a CMOS inverter.

8. (original) A level converter as in claim 7, wherein said first buffer is a CMOS inverter.

9. (original) A level converter as in claim 7, wherein said first buffer is a logic gate.

10. (original) A level converter as in claim 7, wherein said logic gate is a NAND gate.

11. (currently amended) A level converter as in claim 7 [[5]], wherein said CMOS inverter includes an NFET having a threshold higher than other NFETs in said level converter.

12. (currently amended) A voltage level converter circuit comprising:

a first inverter with a first inverter input, a first inverter output, a first inverter ground connected to a circuit ground, and a first inverter voltage supply;

a threshold drop element connected between a circuit high voltage supply (V_{ddh}) and the first inverter voltage supply;

a second inverter with a second inverter input connected to the first inverter output, a second inverter output, a second inverter ground connected to the circuit ground, and a second inverter voltage supply connected to V_{ddh} ~~the circuit high voltage supply~~; and

a voltage feedback element connected between V_{ddh} ~~the circuit high voltage supply~~ and the first inverter voltage supply, the voltage feedback element having an input connected to the second inverter output, wherein when the second inverter output is low ~~has a low value~~, the voltage feedback element causes the first inverter voltage supply to approach V_{ddh} and making ~~the value of the circuit high voltage supply to make~~ the first inverter output approach V_{ddh} [[high]] thereby eliminating a standby power in the second inverter, and wherein when the second inverter output is high, standby power is substantially eliminated in the first inverter.

13. (currently amended) A voltage level converter circuit, as in claim 12, wherein the threshold drop element provides the first inverter voltage supply with a lower voltage than the circuit high voltage supply when the first inverter input is high~~, whereby standby power is substantially eliminated in the first inverter~~.

14. (original) A circuit, as in claim 13, wherein the threshold drop element is at least one transistor.

15. (original) A circuit, as in claim 14, wherein the transistor is a field effect transistor (FET).

16. (original) A circuit, as in claim 15, wherein at least one FET is a plurality of FETs.

17. (currently amended) A circuit, as in claim 15 [[14]], where the FET is a high threshold voltage FET.

18. (original) A circuit, as in claim 13, where the threshold drop element is a diode.

19. (currently amended) An integrated circuit (IC) comprising:

a plurality of circuit rows;

at least one low voltage island in at least one of said plurality of circuit rows, circuit elements in each said at least one low voltage island being powered by a low voltage (V_{ddl}) supply; and

at least one high voltage island in said at least one of said plurality of circuit rows, circuit elements in each said at least one high voltage island being powered by a high voltage (V_{ddh}) supply, V_{ddh} being a higher voltage than V_{ddl}; and,

at least one level converter comprising:

a first buffer receiving an input signal from said at least one low voltage island, said first buffer being connected between a virtual supply and a supply return;

a second buffer receiving an output of said first buffer and connected between V_{ddh} and said supply return; and

a supply select between V_{ddh} and said virtual supply ~~return~~, said supply select receiving an output from said second buffer and selectively passing V_{ddh} or a reduced supply voltage to said virtual supply [[line]] responsive to said output from said second buffer ~~output~~.

20. (original) An IC as in claim 19, wherein said second buffer is an inverter.

21. (original) An IC as in claim 19, wherein said supply select is a supply switch in parallel with at least one diode, both connected between said first supply and said virtual supply.

22. (original) An IC converter as in claim 21, wherein said supply switch is a field effect transistor (FET) gated by said output of said second buffer and said at least one diode is a diode connected FET.

23. (original) An IC as in claim 22, wherein said supply switch FET is a P-type FET (PFET) and said at least one diode connected FET an N-type FET (NFET) diode.

24. (original) An IC as in claim 23, wherein said at least one diode connected NFET is a pair of series connected NFET diodes.

25. (original) An IC as in claim 23, wherein said second buffer is a CMOS inverter.

26. (original) An IC as in claim 25, wherein said first buffer is a CMOS inverter.

27. (original) An IC as in claim 25, wherein said first buffer is a logic gate.

28. (original) An IC as in claim 25, wherein said logic gate is a NAND gate receiving a plurality of V_{ddl} inputs.

29. (currently amended) An IC as in claim 25 [[23]], wherein said CMOS inverter includes an NFET having a threshold higher than other NFETs in said level converter.

30. (currently amended) An IC as in claim 19 [[18]], wherein said reduced supply voltage is below V_{ddl}.